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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,931	03/19/2004	Masaaki Yoshida	R2184.0307/P307	6728

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EXAMINER	
MENZ, DOUGLAS M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,931	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Douglas M. Menz	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *9-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04, 7/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I, claims 1-8, in the reply filed on 12/30/04 is acknowledged. The traversal is on the ground(s) that both groups can be examined without imposing a serious burden on the Office. This is not found persuasive because it has been shown in the restriction requirement filed 12/8/04 that two distinct inventions are claimed which correspond to different classifications in the art i.e. a device and a method of manufacturing.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirase (US 6107672).

Regarding claim 1, Hirase discloses a semiconductor device comprising:

a substrate(1, Figs 1 and 4); and

more than three kinds of wells (3-7, Figs.1, 4 and Col. 4 and Col. 8) formed in said substrate,

wherein one kind of well (4) from among the more than three kinds wells has a surface level higher than other kinds of wells from among the more than three kinds of wells; said one kind of well (4) is formed adjacent to and self-aligned to at least one kind of well (6) from among said other kinds wells; and said other kinds of wells are different in one of a conductivity type, an impurity concentration and junction depth, and include at least two kinds of wells having the same surface level (Figs.1, 4 and Col. 4 and Col. 8).

Regarding claim 2, Hirase further discloses wherein said other kinds of wells (3,5,6 and 7) include more than two kinds of wells having different impurity concentrations to each other (Figs.1, 4 and Col. 4 and Col. 8).

Regarding claim 3, Hirase further discloses wherein at least one kind of well from among said other kinds of wells has an impurity concentration that is decreased to a level necessary to form a high- voltage transistor (Figs.1, 4 and Cols. 4-5 and Cols. 8-9).

Regarding claim 4,Hirase further discloses wherein said other kinds of wells (3,5,6 and 7) include more than two kinds of wells having different junction depths to each other (Figs.1, 4 and Cols. 4-5 and Cols. 8-9).

Regarding claim 5, Hirase further discloses wherein one of said other kinds of wells (3,5,6 and 7) having a larger depth includes a triple well in which a well of an opposite conductivity type having a smaller junction depth is formed (Figs.1, 4 and Cols. 4-5 and Cols. 8-9).

Regarding claim 6, Hirase further discloses wherein said one kind of wells (4) and said other kind of wells (3,5,6 and 7) are of different conductivity types to each other (Figs.1, 4 and Cols. 4-5 and Cols. 8-9).

Regarding claim 7, Hirase further discloses wherein a MOS transistor is formed by a drain diffusion layer and a source diffusion layer formed in the more than three kinds of wells (3,4,5,6 and 7) and a gate electrode formed on areas corresponding to the drain diffusion layer and the source diffusion layer via a gate insulating film (Figs.1, 4 and Cols. 5-6 and Cols. 9-10).

Regarding claim 8, Hirase further discloses wherein MOS transistors are formed by drain diffusion layers and source diffusion layers formed in the more than three kinds of wells (3,4,5,6 and 7) and gate electrodes formed on areas corresponding to the drain

diffusion layers and the source diffusion layers via a gate insulating film, and wherein one of the MOS transistors formed on the triple well is one of a MOS transistor constituting a power supply circuit, a MOS transistor constituting a circuit sensitive to a substrate noise and a MOS transistor constituting a circuit generating a noise (Figs.1, 4 and Cols. 5-6 and Cols. 9-12).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following US patents all disclose semiconductor device structures which incorporate more than three kinds of wells formed in a substrate: 4907058, 4965215, 5159427, 5319236, 5726475 and 6043534.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M. Menz whose telephone number is 571-272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DM

B. WILLIAM BAUMEISTER
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